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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,173	12/19/2001	Masashi Yamaura	H-1020	1355

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,173	YAMAURA ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/15/2003 has been entered.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 01/10/2001. The certified copy of the priority document has been received.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1 recites the limitation "wiring substrate" in line7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 3 and 5-10 are rejected under 35 U.S.C. 103(e) as being unpatentable over Moriyama (US 6,195,260) in view of Seino et al. (US 4,785,533).

9. Regarding claims 1 and 6 (as understood), Moriyama (e.g. fig. 3) shows a semiconductor device comprising:

- Surface mounted parts (6);
- A first substrate 3 on which the surface mounted parts are mounted by first soldering;
- Solder connection portions 7 for connecting the surface mounted parts to the first substrate;

- And a sealing portion 8 formed with an elastic insulative resin (e.g. silicone resin) for covering the surface mounted part (col. 3/lls. 47-49).

10. Although Moriyama does not explicitly teaches that the silicone resin has a modulus of elasticity of 1 to 200 MPa at a temperature of 150°C or higher this is considered an inherent property of silicone resin. Note that silicone is an elastomer that inherently has a modulus of elasticity. Moriyama does not explicitly disclose that the semiconductor device is mounted on a second substrate by a second soldering. Seino (e.g. fig. 1) shows a semiconductor device 3/2 mounted on a second substrate 1 by a second soldering 5. As it is well known in the art, electronic equipment (i.e. computer) comprises many electric devices mounted on a secondary substrate or motherboard (col. 1/lls.21-40). The motherboards are used as a supporting substrate and as an interconnecting means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the semiconductor device disclosed by Moriyama on a second substrate by a second soldering as suggested by Seino in order to provide a supporting means and to interconnect the device into an useful electronic equipment.

11. Regarding claim 3, Moriyama discloses that the elastic insulative resin is a silicon resin (col. 3/lls. 47-49). Although Moriyama does not explicitly teaches that the silicone resin has a modulus of elasticity of 1 to 200 MPa at a temperature of 25°C, this is considered to be an inherent property of silicone resin.

12. Regarding claim 5, Moriyama (e.g. fig. 3) shows a semiconductor device comprising:

- Surface mounted parts (6);
- A wiring substrate 3 on which the surface mounted parts are mounted by first soldering;
- Solder connection portions 7 for connecting the surface mounted parts to the wiring substrate;
- And a sealing portion 8 formed with silicone resin that is an elastic insulative resin for covering the surface mounted parts and the solder connection (col. 3/lls. 47-49).

13. Although Moriyama does not explicitly teaches that the silicone resin has a modulus of elasticity of 1 to 200 MPa at a temperature of 150°C or higher this is considered to be an inherent property of silicone resin. Note that silicone is an elastomer that inherently has a modulus of elasticity. Moriyama does not explicitly disclose that the semiconductor device is mounted on a second substrate by a second soldering. Seino (e.g. fig. 1) shows a semiconductor device 3/2 mounted on a second substrate 1 by a second soldering 5. As it is well known in the art, electronic equipment (i.e. computer) comprises many electric devices mounted on a secondary substrate or motherboard (col. 1/lls.21-40). The motherboards are used as a supporting substrate and as an interconnecting means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the semiconductor device disclosed by Moriyama on a second substrate by a second soldering as suggested by Seino in order to provide a supporting means and to interconnect the device into an useful electronic equipment.

14. Regarding claims 1 and 7, Moriyama (e.g. fig. 3) shows a semiconductor device comprising:

- Surface mounted parts (6);
- A wiring substrate 3 on which the surface mounted parts are mounted;
- Solder connection portions 7 for connecting the surface mounted parts to the wiring substrate;
- And a sealing portion 8 formed with an elastic insulative resin (e.g. epoxy resin) for covering the surface mounted part (col. 3/lls. 47-49).

15. Although Moriyama does not explicitly teaches that the epoxy resin has a modulus of elasticity of 1 to 200 MP at a temperature of 150°C or higher this is considered to be an inherent property of epoxy resin. Note that epoxy resin is an elastomer that inherently has a modulus of elasticity. Moriyama does not explicitly disclose that the semiconductor device is mounted on a second substrate by a second soldering. Seino (e.g. fig. 1) shows a semiconductor device 3/2 mounted on a second substrate 1 by a second soldering 5. As it is well known in the art, electronic equipment (i.e. computer) comprises many electric devices mounted on a secondary substrate or motherboard (col. 1/lls.21-40). The motherboards are used as a supporting substrate and as an interconnecting means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the semiconductor device disclosed by Moriyama on a second substrate by a second soldering as suggested by Seino in order to provide a supporting means and to interconnect the device into an useful electronic equipment.

16. Regarding claim 8, Moriyama (e.g. fig. 3) shows a semiconductor device comprising:

- Semiconductor chips 6 which are surface mounted parts each formed with a surface electrodes main surface, having chips parts which are surface mounted parts each formed with connection terminals on both ends.
- A module substrate 3 which is wiring substrate on which the semiconductor and the chip parts are mounted by a first soldering;
- Solder connections potions 7 for connecting the chip parts to the wiring substrate;
- And a sealing portion 8 formed with silicone resin that is an elastic insulative resin for covering the semiconductor (col. 3/lls. 47-49).

17. Although Moriyama does not explicitly teaches that the silicone resin has a modulus of elasticity of 1 to 200 MPa at a temperature of 150°C or higher this is considered to be an inherent property of silicone resin. Note that silicone is an elastomer that inherently has a modulus of elasticity. Moriyama does not explicitly disclose that the semiconductor device is mounted on a second substrate by a second soldering. Seino (e.g. fig. 1) shows a semiconductor device 3/2 mounted on a second substrate 1 by a second soldering 5. As it is well known in the art, electronic equipment (i.e. computer) comprises many electric devices mounted on a secondary substrate or motherboard (col. 1/lls.21-40). The motherboards are used as a supporting substrate and as an interconnecting means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the semiconductor device disclosed

by Moriyama on a second substrate by a second soldering as suggested by Seino in order to provide a supporting means and to interconnect the device into an useful electronic equipment.

18. Regarding claims 9 and 10, Moriyama (e.g. fig. 3) shows a semiconductor device comprising:

- Semiconductor chips 6 which are surface mounted parts each formed with a surface electrodes at its main surface, having chips parts which are surface mounted parts each formed with connection terminals on both ends.
- A module substrate 3 which is wiring substrate on which the semiconductor and the chip parts are mounted by a first soldering;
- Solder connections potions 7 for connecting the chip parts to the wiring substrate;
- And a sealing portion 8 formed with epoxy resin that is an elastic insulative resin for covering the semiconductor chips, the chip parts and the solder connection portions (col. 3/lls. 47-49).

19. Although Moriyama does not explicitly teaches that epoxy resin has a modulus of elasticity of 1 - 200 MPa a temperature of 150°C or higher and a modulus of elasticity of 200 MPa or more at a temperature of 25°C a this is considered to be an inherent property of the epoxy resin. Note that epoxy resin is an elastomer that inherently has a modulus of elasticity. Moriyama does not explicitly disclose that the semiconductor device is mounted on a second substrate by a second soldering. Seino (e.g. fig. 1) shows a semiconductor device 3/2 mounted on a second substrate 1 by a second

soldering 5. As it is well known in the art, electronic equipment (i.e. computer) comprises many electric devices mounted on a secondary substrate or motherboard (col. 1/lls.21-40). The motherboards are used as a supporting substrate and as an interconnecting means. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the semiconductor device disclosed by Moriyama on a second substrate by a second soldering as suggested by Seino in order to provide a supporting means and to interconnect the device into an useful electronic equipment.

20. Claim 11 is rejected under 35 U.S.C. 103(e) as being unpatentable over Moriyama (US 6,195,260) in view of Seino et al. (US 4,785,533) further in view of Ishida (US 6,329,065).

21. Regarding claim 11, Moriyama in view of Seino discloses most aspects of the instant invention. However, Moriyama does not disclose that the terminals are plated with gold, tin or lead-tin alloy. Ishida discloses that the surface of the surface wiring layer may be provided with a plated layer based on nonelectrolytic plating, electrolytic plating or the like method in order to prevent corrosion caused by oxidation, to improve wire-bonding property, to improve wettability to the solder and to decrease the electric resistance. Examples of the metal for forming such a plated layer include Au, Cu, Ti, Ni and Pd. In particular, it is preferable that the most front surface of the plated layer is formed of Au (col. 5/lls. 45-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to plate the surface of the wiring layer disclosed by Moriyama with gold in order to prevent order to prevent corrosion caused

by oxidation, to improve wire-bonding property, to improve wettability to the solder and to decrease the electric resistance as taught by Ishida.

22. Claims 12 and 14 are rejected under 35 U.S.C. 103(e) as being unpatentable over Moriyama (US 6,195,260) in view of Seino et al. (US 4,785,533) further in view of Ishida (US 6,329,065) further in view of Wolf et al.

23. Regarding claim 12, Moriyama (e.g. fig. 6) in view of Seino further in view of Ishida shows most aspects of the instant invention including surface electrodes of a semiconductor chips that are wire bonded to the substrate. Moriyama does not disclose the wiring material. Nevertheless, it is well known in the art that gold and aluminum are the most used materials in the wire bonding technology. Wolf discloses that gold is a common wire bonding material since gold is highly conductive and ductile enough to withstand the deformation during the bonding steps (page 852, 1st paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the wires disclosed by Moriyama in view of Ishida of gold since gold is highly conductive and ductile enough to withstand the deformation during the bonding steps as taught by Wolf.

24. Regarding claim 14, Moriyama shows that the semiconductor chips and the chip parts are mounted on a rectangular module substrate 59. Also, the wire loops are formed in a direction parallel to the longitudinal direction of the module substrate.

25. Claims 13 is rejected under 35 U.S.C. 103(e) as being unpatentable over Moriyama (US 6,195,260) in view of Seino et al. (US 4,785,533) further in view of Ishida (US 6,329,065) further in view of Zakel et al (US 5,989,993).

26. Regarding claim 13, Moriyama (e.g. fig. 6) shows that the main surface of the semiconductor chips and the surfaces of the wiring substrate on the side of supporting the chips are opposed to each other. Also, the surface electrode of the semiconductor chips and the substrate terminals are connected by bumps 7 whereas Ishida teaches that the substrate terminals are formed with a gold metal layer. Moriyama does not disclose the bump material. Nevertheless, it is well known in the art the use of gold bump and solder bump as interconnection means. Zakel discloses that solder bumps or gold bumps are commonly used in the flip chip and TAB technology (col. 1/lls. 12-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the bump disclosed by Moriyama in view of Ishida of gold or solder since those are commonly used materials in the flip chip and TAB technology because of its excellent conductive and wettability properties.

Response to Arguments

27. Applicant's arguments filed 12/15/2003 have been fully considered but they are moot in view of a new ground of rejection.

Conclusion

28. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

30. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

31. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/668, 690,702	01/04
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	01/04

Leonardo Andújar
Patent Examiner Art Unit 2826
1/22/2003